

# MAXIMISING YIELD **in high- frequency circuits**

By Josh Moore

**A** key goal in the development of a microwave monolithic integrated circuit (MMIC) is to ensure maximum yield of the circuits against a set of post-fabrication tests. Overall yield is affected by a variety of factors but a key element is parametric yield, or yield variation due to modelling inaccuracies and process parameters that vary significantly on different circuits fabricated over the production lifetime. Fortunately, electronic design automation (EDA) tools can help the high-frequency designer tremendously in determining the severity of parametric effects on yield. The yield-analysis capabilities of EDA software are powerful enough, and easy enough to use, that

it is more practical to consider parametric yield effects as one of the performance targets from the initial stages of a design, rather than to leave them as an afterthought that is only explored after the design is finished.

Parametric yield prediction in EDA tools can provide valuable insight into relative trends due to parametric variations, but often does not provide an absolute indication of production yield. The main reason is that only a finite number of effects can be characterised by any simulation model. For example, problems such as unintended coupling can lead to performance issues that were not considered in the simulation. As with any high-frequency simulation, this places the responsibility of developing a good EDA tool →



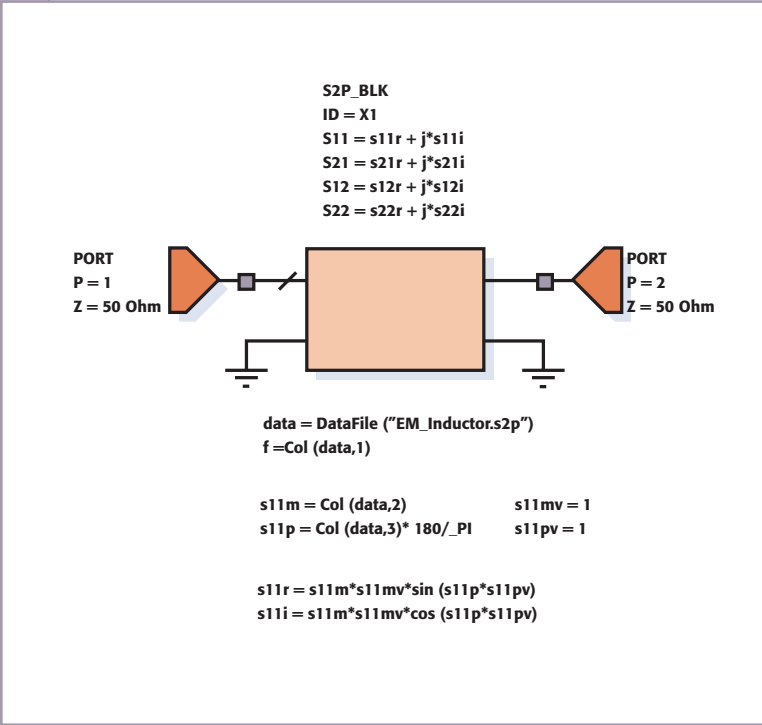


Fig 1: Electromagnetic stimulation setup for analysing the statistical variance of an inductor using a mathematical function

representation of the circuit and an understanding of the variances that take place within the circuit on the designer.

There is a three-step yield simulation process that can be used to achieve accurate results. The first step is to quantify both the parameters that vary over the production lifetime and the sources of modelling inaccuracy that could affect yield. This can present a challenge, as proper quantification of parametric effects requires very large sample numbers to develop. For example, in a MMIC process, the distribution of etch depths for pseudomorphic high electron mobility transistor (pHEMT) gates varies, which results in different pinch-off voltages ( $V_p$ ). Sampling a single wafer, or even wafers spread out over a month of production, might not fully characterise the  $V_p$  variation. Good MMIC foundries understand this and constantly sample and adjust statistical parameters over the lifetime of a process. This ensures that, for a mature process, the foundries are able to provide end users with excellent parametric variation data. Examples of parametric variation for a printed circuit board are the manufacturer's component value tolerances for surface mount technology parts.

Finally, an example that is common to almost any high-frequency fabrication process is the etch tolerance on the metallisation and substrate deviations that can occur. As with  $V_p$  for a FET-based MMIC, good characterisation of these effects, especially substrate variation, can require large sample sizes for high accuracy. These effects are often the

RF designs are highly susceptible to parametric yield effects



most difficult to use in a simulation when electromagnetic (EM) modelling is used for many of the passive structures.

In order to understand the difficulty, first consider how parametric parameters are entered into EDA simulations once they have been quantified. Typically, they are added as properties on the various models, with the user having controls that describe the variation as a percentage of the mean value or as the addition and subtraction from the mean value. Other settings might include the type of statistical distribution that each parameter has. For a traditional high-frequency model, such as a microstrip line model, and its substrate definition, the parametric effects are easily applied. However, modern designs are rarely straightforward. Advances in simulation technology and computer speed have made using EM analysis for significant portions of the circuit a reality.

### STATIC MODELS

EM is commonly used to model for inductors, coupled circuit sections, distributed line junctions and so on. These models are more static than closed-form models in that they require a time-consuming – that is, minutes or hours – re-simulation to quantify any change that occurs to the physical structure or dielectric stackup. As a result, performing successive yield analysis simulations is a daunting task, which, in effect, leaves the designer with a set of process variations that are difficult to quantify.

“ Any performance metric that can be simulated with EDA can be considered as part of yield analysis ”

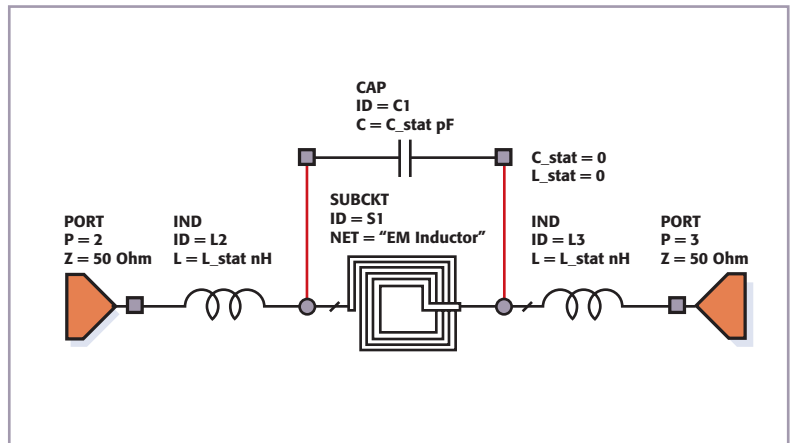


Fig 2: Electromagnetic simulation results setup for analysing the statistical variance of an inductor with circuit-simulation elements

From a practical perspective there are several ways a designer can approach this problem. One way is to allow the S-parameters from EM simulations to vary with a mathematical function that contains a statistical parameter, as shown in fig 1. In this case, the data from an EM simulation is read in (s11m) and multiplied by a modifier (s11mv), which is set up to have a mean value of 1 with a deviation of  $\pm 2\%$  deviation.

The key to this technique is that the nominal value of the multiplier will not effect the simulation, but during yield analysis the results are perturbed. This approach is simple to set up, but it can be challenging to come up with a mathematical formula that captures the relationship between S-parameters and the varying physical quantity or modelling uncertainty.

**SIMULATION WRAPPING**

Another approach is to ‘wrap’ the EM simulation results with traditional high-frequency models as shown in fig 2. For example, both the parametric variations and modelling errors of a high-frequency inductor that was modelled with EM simulation can be accounted for by the addition of lumped element components. In fig 2, the series capacitor added across the EM inductor represents the modelling error caused by using a 2.5D EM simulator that does not fully account for sidewall capacitance. The series capacitor has a nominal value of 0pF and a statistical variance of  $\pm 1.1\text{fF}$ . The series inductors on the pins of the EM inductor represent the uncertainty in the phase through the structure. These inductors are tied together, and have a nominal value of 0nH and a statistical variance setting of  $\pm 0.3\text{ nH}$ , which is 15% of the value of the inductor. This approach to adding statistical variance to EM models has the advantage of using simple, well-understood simulation models to describe the variations. The designer, however, is required to understand the sources of variation and the amount by which they vary.

Once all of the parametric effects and modelling errors are quantified, the second step for yield analysis is to configure yield goals that will be used by the simulator to determine if a given test case passes or fails. The yield goals are described in terms of circuit performance. Any performance metric that can be simulated with EDA tools can be considered as part of yield analysis. This allows the flexibility to look at standard small-signal performance metrics such as gain, noise, stability and return loss.

Today’s EDA tools are fast enough that it’s reasonable, and highly recommended from a design perspective, to monitor important nonlinear results such as active device operating points, saturated output power, power added efficiency, etc. The main goal is to consider all of the performance metrics that will most likely be affected by the parameter-variation setup in the first step and, of course, performance metrics that will be used as the pass/fail criteria on the production line. Ideally, any yield goals are automatically displayed for the designer so, providing a visual reference of the circuit’s performance relative to the metrics, as shown in fig 3.

The final step in predicting yield is performing the →

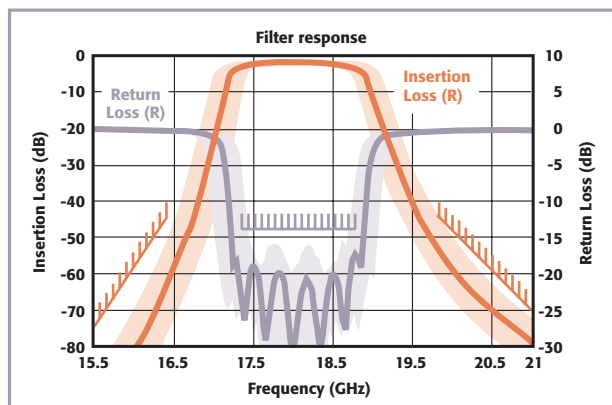


Fig 3: Yield goals with simulated results for a filter

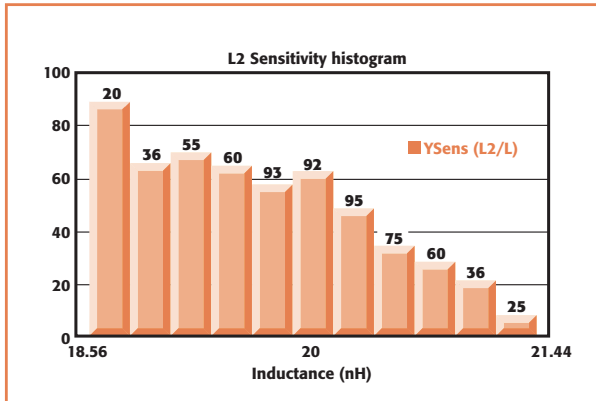


Fig 4: Initial yield sensitivity results for the variation of an inductor in a filter

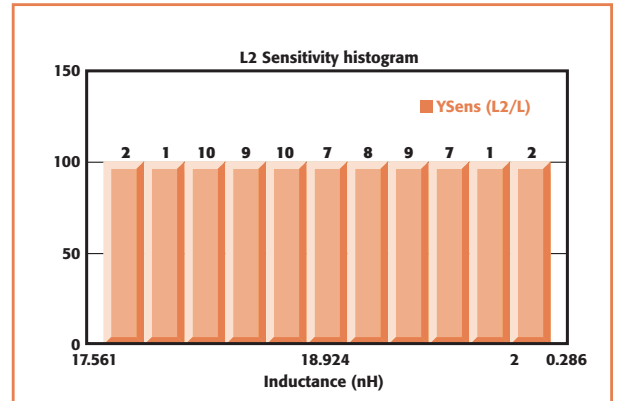


Fig 5: Optimised yield sensitivity results for the variation of an inductor in a filter

actual simulation. Normally, this simulation is considered to be very time-consuming because of the thousands of iterations that are required. The exact formula for the number of iterations required for a given confidence level in the results is:

$$N = (C_0/\epsilon)^2 * Y * (1 - Y)$$

In this formula, N is the number of required trials, C<sub>0</sub> is the desired confidence level expressed in terms of standard deviations (a C<sub>0</sub> of 2 corresponds to a confidence level of 95.4%), ε is the percentage error on the calculated yield and Y is the estimated yield, which can be calculated with a short yield analysis simulation comprising 20-30 trials. Working through the math shows that for a 75% yield, calculated with a 95% accuracy with 1% error, requires 7500 simulations. However, if the error percentage is increased from 1% to 5%, then the number of required trials is reduced to 300, which takes about 25 seconds to simulate with modern EDA software running on a 1.6 GHz Pentium IV with 512MB of memory. Clearly, this simulation iteration reduction presents a significant time saving to the end-user and makes it reasonable to perform multiple yield trials while tweaking the goals, parametric variations, and component values. From a practical perspective, the decrease in accuracy from 1% to 5% is probably negligible in light of the relative nature of simulated yield and the circuit tweaks that fast simulations allow the end-user to make in order to improve the performance.

The end goal of all yield simulations is to maximise the yield. After the simulation is finished, EDA tools provide several aids to help designers in this goal so they are not left to randomly make changes to their circuit and hope for improvements. The first of these is yield sensitivity, or how many of the failures were due to a parameter having a particular value based on its statistical distribution. Yield sensitivity plots, as shown in fig 4, are usually viewed as histograms with component value on the x-axis and percent yield on the y-axis. In addition, each bar in the histogram is labelled with the actual number of yield failures due to a

given range of component values. Fig 4 shows the yield sensitivity of a filter due to the statistical variation of one of the inductors (L2) in the circuit. Looking at the graph, it can be seen that the inductor has a mean value of 20nH and is set up to vary by roughly ±7.5%. The most important detail of the graph is the shape of the histogram. For this inductor, values that are lower than the nominal value result in a high yield. Values that are higher than the nominal value cause a lower yield. The non-uniform nature of the distribution shows that the design is sensitive to this part, which in turn leads to the conclusion that, while this part may be optimally chosen for nominal performance, it isn't particularly well-chosen when manufacturer variation is taken into account. These challenges are often associated with highly optimised or peaked designs in which the chosen nominal component values give excellent response, but also perch the design on the edge of a cliff in terms of failures.

Ideally, this graph would show a high uniform distribution across all potential inductor values. A uniform distribution indicates that there are roughly the same number of failures associated with any given inductor value, so the overall design is not very sensitive to this component's process variation. In addition, high numbers indicate the overall yield is good. If yield numbers are low with a uniform distribution, this simply indicates that the current component is not a significant contributing factor. After the

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*Reducing sensitivity to variations caused by manufacturing is a key part of yield-aware design*



initial yield analysis is complete and the sensitivities to all of the process variations are explored, a clear picture of which effects are significant contributors to failures begins to emerge.

### YIELD ANALYSIS

Discovering problem areas with no clear means to fix them would be an exercise in futility. At this point in a design the designer could manually re-tweak the nominal values for the sensitive components and, due to the fast simulation speed of basic yield analysis, get a quick feel for improvements or degradations that have been made. In all but the simplest cases, however, this task quickly becomes a daunting one, as the interaction between different process variations and the overall effect on the final circuit is a large, multi-dimensional problem space.

For this reason, high-frequency EDA tools provide an analysis capability that allows designers to optimise their design for yield. This is a complex process that involves altering the nominal value of the process variations, analysing the effect on the yield of the circuit, and repeating until an optimum is achieved. Unlike basic yield analysis, this process requires many more iterations. As with any optimisation, the more opportunity it is given to succeed the more likely that it will. The good news is that, unlike regular yield analysis that simply provides results, yield optimisation actually improves circuit performance, so a longer simulation time due to more iterations is well worth it. For the filter circuit previously referenced, where 300 iterations took 25 seconds, 5000 iterations take 6 minutes and 30 seconds. The final result of yield centring is that the component sensitivity is more uniform for each process variation and, as a natural result of that, the overall yield is improved. Both of these effects can be seen in fig 5, which shows the same graph as fig 4 after a 1000-trial yield optimisation process.

In conclusion, high-frequency EDA tools, such as Microwave Office design suite from Applied Wave Research,



*Optimising yield is vital for high-volume RF markets such as radio tags*

which was used for this example, provide designers with the ability to set up and analyse all known parametric effects on circuit yield. This enables them to understand which effects have the most impact on their designs, and to centre the designs in light of the known issues. These powerful analysis techniques are not intended to be used simply at the end of the design cycle, but as an integral part of the entire design process, thereby helping designers to meet both the desired performance and the parametric yield effects for their circuit. Treating yield as an additional performance goal that is taken into account from the early stages of a design makes the process of accounting for yield much easier in the long run, and reduces the stress that results from being forced to fix yield issues at the end of a design in a way that may impact nominal circuit performance. ■

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