

Summit Semiconductor cuts the design time for 10GHz phase shifter and low noise amplifier products in half with Analog Office

Customer Background

Summit Semiconductor provides design services and licenses intellectual property (IP) for silicon germanium (SiGe) and gallium arsenide (GaAs) integrated circuits (ICs) for RF, microwave, and millimeter-wave applications. The company addresses a need for experienced IC development from initial concept to final product, including backend processes.

Summit Semi allows customers to choose from several product development solutions. For ICs, it provides full development from system level partitioning to IC design, layout and foundry tape out. Summit Semi backend process services include packaging, assembly and test. This allows it to provide complete product development solutions from IC design to guiding the customer's product through qualification, providing failure analysis as needed, and developing/managing the supply chain for volume production. Summit Semi has provided IC solutions for military, wireless, satellite, and communication systems.

Customer:

Summit Semiconductor

Application:

RF, microwave and millimeter-wave integrated circuits

AWR Products:

Analog Office® Design Suite

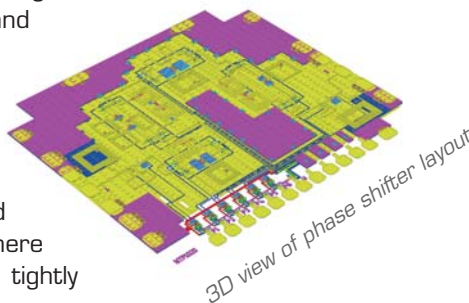


The Design Challenge

Summit Semiconductor, a design services company under contract to develop 10GHz phase shifter and low-noise amplifier products for a major customer in the wireless marketplace, had several design challenges. This complicated new IC chip set was an important new product line for the customer.

The phase shifters were critical for beam steering functions in phased-array radar and commercial communication systems. The low-noise amplifiers provide gain blocks with moderate noise figure.

The frequency range, along with noise and gain specification, required accurate device and transmission line models for circuit simulation in both time and frequency domains. In addition to the challenges of line and inductor coupling, electromagnetic (EM), skin effect, and interconnect coupling and extraction, there were issues with having a dense layout tightly coupled with the circuit implementation.



The design environment had to be simple, user-friendly, and intuitive, yet support all the design functionalities and features required to tape out on an accelerated schedule. In order to meet the architecture, circuit design, layout, and physical verification challenges, the design environment had to be comprehensive, could not require a major CAD support team, and had to provide interfaces to third-party design tools.



"We have chosen to standardize on Analog Office from Applied

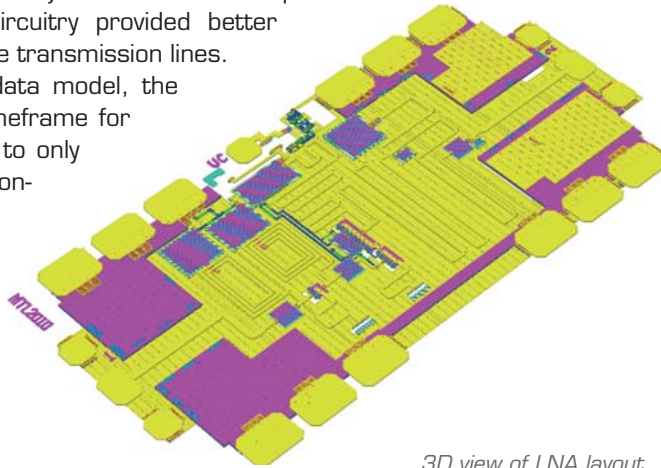
Wave Research for all our analog IC design. Our design engineers are especially excited about the accuracy of the device models, 3D visualization of the IC layout, and the integration of layout with simulation."

Rick Sturdivant
President
Summit Semiconductor
www.summitsemi.com

The Solution

AWR's Analog Office software, with its ease-of-use, accurate device models, and fully integrated design environment with advanced layout and simulation capabilities tied together with the schematic, helped the Summit Semiconductor design team to significantly reduce its design cycle time. The team was able to go from specification to tapeout in half the time. The ability to perform "on-the-fly" extraction at any point in the design cycle enabled the design team to accurately simulate interconnect parasitics along with line coupling physical effects early in the circuit design phase. This methodology coupled with utilizing the optimization and tuning capabilities enabled the Summit design team to develop the best topology for its circuit and matching layout.

The ability to mix and match a variety of simulation techniques on different parts of the circuitry provided better analysis of the behaviors of the transmission lines. With AWR's unique unified data model, the typical seven-to-eight-week timeframe for designing the layout was cut to only three weeks. The verification-to-foundry design checks were performed using the Analog Office design rule check (DRC) interface, which highlights errors in the layout itself, enabling correction early in the process and saving design time.



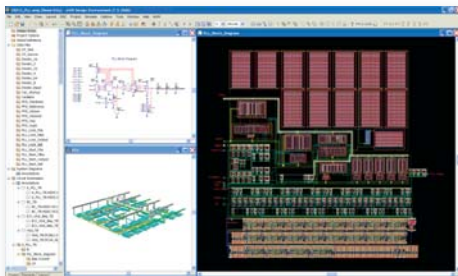
3D view of LNA layout

"The integrated design environment delivered quicker time to market for our customers and reduced our development costs significantly."

Rick Sturdivant
President
Summit Semiconductor
www.summitsemi.com

Product Overview

The Analog Office design suite is the first complete design system that is specifically architected and optimized from the ground up for next-generation radio-frequency integrated circuit (RFIC) designs. Much more than a point tool, the Analog Office integrated environment boasts an industry-first, concurrent interconnect-driven and RF-aware design methodology that delivers unprecedented interactivity, and accuracy. The solution is built on AWR's open high-frequency design platform. The Analog Office design suite enables analog and RFIC design engineers to significantly shorten their development cycles and speed wireless products to market.



Analog Office 2007 software provides higher capacity and faster layout for mixed-signal design, such as this complex phase-locked loop



AWR is a member of Silicon Integration Initiative (Si²) and OpenAccess Coalition (OAC)



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