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RF EDA moves from niche to mainstream

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RF EDA has been around for a long time, in the form of microwave component PCB and monolithic microwave integrated circuit (MMIC) tools. Drivers for this market include aerospace, satellite communications, high-speed optical, wireless infrastructure, and power amplifiers products operating in the gigahertz range. These products are primarily built in compound semiconductor technologies such as gallium arsenide (GaAs), indium phosphide (InP), and silicon germanium (SiGe).

Traditional RF EDA tools for this market include harmonic balance, periodic steady-state, and electromagnetic (EM) simulation. By measures based on the EDA Consortium (EDAC) Market Statistics Report [1] and other market data sources, the total revenues for these tools ranged from \$120 million to \$150 million in 2003. And consistent with what has been experienced in the overall electronics industry, this market has been under pressure over the last several years.

While some RF EDA industry leaders may have posted lower earnings numbers recently, there are also many start-ups and up-and-coming new players in the market who have introduced compelling new technologies to meet the demands of today's complex products. These new players have enjoyed success and steady growth even in this uncertain economy. Their presence and success are clear indicators of both the health of this industry segment, and the driving need for new RF EDA technology and methodology to address current design problems.

Looking forward, one only needs to observe the explosive growth of the wireless market and its dependence on RFICs to understand the critical and increasing need for RF EDA. There is a resurgence of the traditional markets driving microwave/RF EDA, as evident in the new expansion in aerospace, cellular, wireless local area network (LAN) and global positioning satellite (GPS). New applications such as ultra-wideband (UWB) wireless and collision avoidance are contributing as well.

Brian Matas, vice president of market research for IC Insights, expects the associated compound semiconductor market will more than double to \$4.4 billion in 2008, growing an impressive 16 percent annually [2]. Sean Maloney, Intel executive vice president and general manager of the Intel Communications Group, stated at the January 2004

Wireless Communications Association (WCA) annual symposium that WiMAX-certified systems will provide the building blocks to connect the next five billion users to the Internet and truly usher in the broadband wireless revolution [3]. These dynamics are fueling new advances and growth in the RF simulation segment and the broader microwave/RF EDA solution market.

The force driving even greater growth in RF EDA is the rapid and increasing integration of high-frequency radios into silicon RFICs. IC Insights reports that the overall wireless IC market (of which RFIC is a significant component) reached \$22 billion in 2003 and grew 25 percent over 2002. They predict it will continue to grow faster than the overall semiconductor market, which is forecast to grow 15 percent year over year [4].

As a consequence of this drive toward semiconductor integration, the industry is now seeing full RF transceiver systems on a single chip for applications like wireless fidelity (Wi-Fi), 802.11a,b,g, and cellular that use cost-effective RF complementary metal oxide semiconductor (CMOS) and bipolar CMOS (BiCMOS) processes. These RF system-on-chip (SoC) solutions can no longer be prototyped or bread-boarded and must be validated before expensive and lengthy mask and wafer fabrication. Because of the integrated nature of these RF SoCs and their performance dependency on the layout and package, designers can no longer decouple system and circuit or electrical and physical design without experiencing numerous product spins and costly delays.

Achieving "RF closure" across the system and circuit electrical and physical design process is crucial for timely product market entry. Existing decoupled IC and package electrical and physical EDA tools with disparate databases and use models are inadequate for meeting these modern design requirements. A much more tightly integrated and physically aware EDA platform built upon a unified data model is essential. A platform that can handle the complexity of these large RF SoCs in the context of the package is also important.

The demands of RF closure dramatically expand the size of the RF EDA market. Harmonic balance, periodic steady-state, and EM simulation are just a few of the many specialized tools needed to verify the complex behavior of RFICs in a package. System simulators and libraries tailored to RF applications are needed to predict system-level transceiver figures-of-merit such as adjacent channel power ratio (ACPR) and bit error rate (BER).

For RF, it is important to simulate these performance figures in the presence of non-ideal circuit impairments that include noise, amplifier compression, and phase shift. Time-domain circuit and mixed-signal simulators utilizing high-frequency active and passive models for SiGe bipolar, RF CMOS, inductor components, and even transmission lines, are needed. Mixing frequency and time-domain analysis should be seamless and intuitive.

The interconnect, substrate, and package parasitics must be considered. Important parasitics include resistance and self/coupled capacitance/inductance, as well as transmission line effects for long and large interconnect and substrate areas. EM and

exotic parasitic extractors are required to calculate these parasitic models.

In some cases, thermal effects must be comprehended in circuits like power amplifiers. The layout editor must be unified for chip-in-package design and must be RF aware and tightly coupled to the simulators and schematics. Circuit optimizers, placers, routers, and compactors that handle RF constraints will be used.

Even design rule check (DRC), electrical rule check (ERC), layout vs. schematic verifier (LVS), and mask-making tools will be extended to handle the peculiar needs of high-frequency design. Therefore, as the tools in the high-frequency design process become more specialized, they all must be considered when sizing the overall RF EDA opportunity. Including these tools greatly expands the scope and size of this market.

By itself, the proliferation of RF SoCs will no doubt accelerate and expand the growth of RF EDA. However, it is the increasing speed of semiconductor products in general, both analog and digital, that will drive these same tools and methods into all areas of high-performance circuit design. Optical and Ethernet transceivers, gigahertz clocks and phase lock loops (PLLs), high-speed digital input/outputs (I/Os), and data converters all require the same intimate coupling of electrical and physical design.

In other words, all custom IC design will employ RF EDA tools and methods in the future, with the exception of those few applications where frequencies are much lower, such as power management circuits and instrumentation amplifiers. The entire high-performance custom IC EDA market (by EDA Consortium measures, well over \$500 million and expanding [1]) will be fertile ground for RF tools and methods.

The last several years have been challenging for the entire electronics industry, including EDA. With the decline in R&D investment since the bubble economy of the late 1990s, it is hard to find strong growth in any segment of the EDA market, no matter how narrowly it is defined. The semiconductor industry, however, has recently seen its fabs fill to capacity, and, according to a recent Semiconductor Industry Association forecast, growth is again predicted in top line and R&D budgets for several years to come [5].

At a recent EDAC CEO Forecast Panel, the general consensus was that the EDA market would follow the semiconductor recovery by six to 12 months [6]. And as it recovers, there is no doubt that the RF EDA market will grow much faster than the overall market as it expands beyond the narrow simulation niche that defined it in the past. The question that remains is, who are the emerging industry leaders who will solve the many challenges that exist in delivering the next generation of RF EDA solutions?

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