SOLVING FDD COMPLIANCE ISSUES WITH 3GPP LIBRARIES

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The complexity of the Third Generation Partnership Project (3GPP) frequency division duplexing (FDD) signal format imposes new linearity and dynamic range requirements on designers, raising serious compliance issues. Fortunately, new design libraries have been developed to help. Despite talk about the benefits of a time division duplexing (TDD) scheme, initial 3G wideband code division multiple access (W-CDMA) systems will need to be developed using an FDD approach. This is because FDD provides a similar operating format for 3G operators and equipment developers (separate bands for transmit and receive operations), while TDD calls for carriers to abandon traditional approaches and use a single 5 MHz channel for both transmit and receive operations.

While the FDD format is similar in nature to existing cellular approaches, the complexity of an FDD signal format complying with 3GPP specifications imposes new performance requirements for linearity, as well as dynamic range of amplifiers and other RF components. Signal statistics such as ratio of peak power to average power and complementary cumulative distribution function (CCDF) become more important. In addition, it becomes obvious that traditional two-tone tests are not accurate enough to characterize the nonlinearities of an amplifier on measurements such as adjacent channel power ratio (ACPR). To further complicate compliance, 3GPP base station and handset measurements require specific test signals (or test models) for each measurement, including ACPR or adjacent channel leakage ratio (ACLR), error vector magnitude (EVM), spectral emission mask, and output power dynamics.

From an RF/analog engineer's perspective, designing to 3GPP FDD compliance testing becomes much more complicated if they must construct a specific signal, even before an EVM measurement can be made. Although each of the aforementioned topics merits a paper of its own, this article provides an overview of the measurement of EVM or modulation accuracy of a 3GPP FDD base station, and examines how Visual System Simulator™ design software from Applied Wave Research (AWR™) provides a unique solution that meets the needs of an RF/analog engineer in terms of making 3G compliance measurements with minimum effort.

The best method for determining a communication link's quality is to directly measure the bit error rate (BER) by making a comparison of the originally transmitted bits with the received bits, and recording the number of erroneous bits received. The BER is the ratio of the number of bits received in error over the total number of bits sent. To assess the impact of an RF amplifier on a communication link, however, it may not be practical to measure BER. Although driving an RF amplifier into compression will affect BER performance, it is essential to measure the impact the RF amplifier will have on the overall communication system.

Taking this into account, measuring the EVM of an RF device is more common than computing the BER of a signal passing through that device. EVM is a metric used to quantify the difference (in magnitude and phase) between the ideal reference and measured waveforms, and is a reflection of the communication link's modulation accuracy. In essence, the measured waveform is a corrupted version of the reference signal. The distortion of the reference is due, for example, to the nonlinear characteristics of the RF link, noise, frequency offset, amplitude imbalance, and phase imbalance. The difference in the reference and measured signals is the error vector. The constellation plot in Figure 1, a mapping of the in-phase (I) and quadrature (Q) components of a signal, illustrates the error vector and EVM. If the measured signal (z'_n) were perfect, then its I and Q components would fall exactly on that of the reference signal (s_n) and the EVM would be zero.

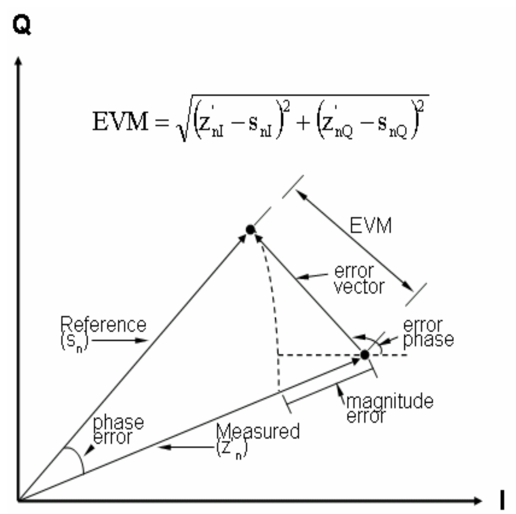

Figure 1: EVM

3GPP standards for an EVM specify that, "Both waveforms pass through a matched Root Raised Cosine (RRC) filter with bandwidth 3.84 MHz and roll-off α = 0.22. Both waveforms are then further modified by selecting the frequency, absolute phase, absolute amplitude, and chip clock timing so as to minimize the error vector. The EVM result is defined as the square root of the ratio of the mean error vector power to the mean reference power expressed as a %. The measurement interval is one timeslot as defined by the C-PICH (when present) otherwise the measurement interval is one timeslot starting with the beginning of the SCH. The requirement is valid over the total power dynamic range[1].”

In other words, the reference and measured signals must pass through RRC filters that have the same bandwidth as the chip rate. An RRC filter is used to reduce the spectral side lobes of a signal. The matched RRC on the measured signal is used to eliminate the intersymbol interference (ISI) introduced by the RRC applied to the reference signal. Next, the impairments induced by the RF link, as mentioned above, must be minimized before the error vector is computed. This can be accomplished using several different methods. In addition, the incoming symbols must be sampled at the correct time.

In the example presented here, we use a downlink “ideal” receiver to detect the common pilot channel (C-PICH) to estimate the phase offset of the RF amplifier and the synchronization channel (SCH) for chip synchronization. This ensures an optimum sampling point of the incoming symbols. The root mean square (RMS) EVM as shown in equation [1] can be measured after the above steps have been taken.

$$\mathrm{EVM}_{\mathrm{RMS}}\% = \sqrt{\frac{\frac{1}{N}\sum_{n\in \mathrm{N}}\left|z_n^{'} - s_n\right|^2}{\frac{1}{N}\sum_{n\in \mathrm{N}}\left|s_n\right|^2}} \times 100 \quad [1]$$

Note that z'_n is a sample of the “corrected” version of the actual measured signal, z_n. The measurement interval is one time slot or 2560 chips (666.6μs), thus the RMS EVM calculation is over blocks of 2560 symbols in length (N = 2560).

In addition to defining the base station conformance tests and their corresponding parameters, the 3GPP specifications also describe the exact signals to use. These reference signals are called “test models.” When measuring EVM at the base station, test models 1, 4, and 5 can be used as the stimulus of the RF link. The key differentiator between the test models’ signals is the number of active channels or dedicated physical channels (DPCH) that are generated. Test model 4 does not have an active DPCH, while test model 1 supports 16, 32, or 64 active channels. The number of DPCHs to be generated is determined by the total number of calls that can be handled by the base station. The spreading code, timing offset and level setting of each DPCH is defined in the specifications so as to simulate a realistic traffic scenario which may have high peak-to-average ratio (PAR). The average power level of the base station is set to its maximum level (P_{MAX}) when test model 1 is employed, and is backed off by 18dB (P_{MAX}-18) when test model 4 is used. Test model 1 is a more stringent test of an RF device’s EVM than test model 4. Test model 4 can be used for testing the digital accuracy of the modulator, which is a higher fidelity measurement of EVM. Earlier versions of the 3G base station conformance tests (up to June 2002) required test model 4 as the only test model for EVM. Obviously, using test model 1 as a replica of a “real world” 3G base station signal gives a greater insight on the EVM measurement of an RF device than using test model 4.

3G conformance tests state that, "the EVM shall be less than 17.5% when the base station is transmitting a composite signal using only quadrature phase shift keying (QPSK) modulation and shall be less than 12.5 % when the base station is transmitting a composite signal that includes 16 quadrature amplitude modulation (16QAM) modulation[2]." The EVM requirement for base stations providing HSPDA is more rigid because a 16QAM constellation is considerably more compact than that of a QPSK, and a higher EVM will result in the detection of more symbols in error.

The October 2003 3G EVM conformance test (release 6) requires that test model 5 be used for 3G base stations supporting high-speed physical downlink shared channel (HS-PDSCH) transmission using 16QAM modulation. The addition of the HS-PDCH to the 3G physical layer is a direct result of the introduction of high-speed downlink packet access (HSDPA), which can potentially offer users 10MB/s data rates in the downlink. Thus, the test model used for conformance testing is determined by which options the base stations can support. Support of test model 1 is mandatory to comply with European Harmonized Standard (ETSI EN 301 908-3)[3]. This article explores the impact of the three configurations of test model 1 on the EVM requirements.

Constructing the necessary test model by writing proprietary code, or from a series of primitive models, is an overwhelming task for engineers not involved in signal processing. The 3G specifications for the test models are complex and highly varied. For example, test model 1 (section 6.1.1.1) is defined in Table 1. As referenced in this table, the Level setting, Channelization Code and Timing offset of the individual DPCHs are found in table 6.2 of section 6.1.1.1.

Type	Number of Channels	Fraction of Power (%)	Level setting (dB)	Channelization Code	Timing offset ($x256T_{chip}$)
P-CCPCH+SCH	1	10	-10	1	0
Primary CPICH	1	10	-10	0	0
PICH	1	1.6	-18	16	120
S-CCPCH containing PCH (SF=256)	1	1.6	-18	3	0
DPCH (SF=128)	16/32/64	76.8 in total	see table 6.2	see table 6.2	see table 6.2

Table 1: Test Model 1 Active Channels

In section 6.1.1.5, the structure of the DPCH and all of the common channels (P-CCHP, C-PICH, SCH) are defined. Figure 2 shows a high-level block diagram of the steps necessary to construct the base station downlink DPCH.

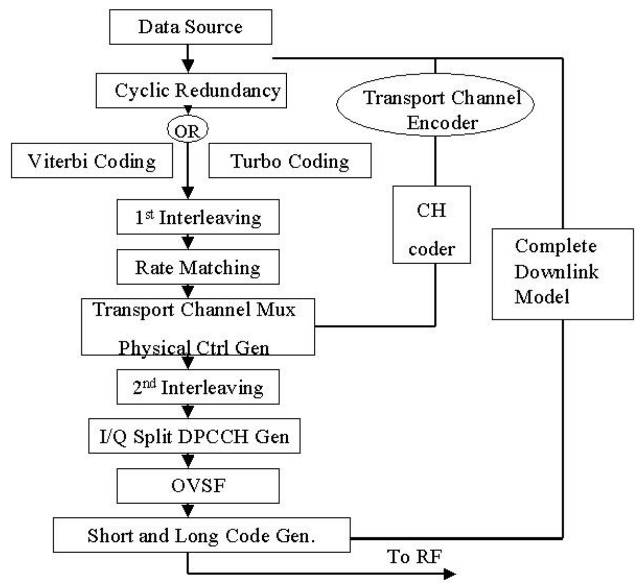

Figure 2: A 3GPP DPCH Signal Generator

Constructing just one DPCH signal from basic building blocks is quite time consuming due to its complexity.

In Figure 3, a pre-configured test model 1 is used to measure the EVM of an RF amplifier circuit design. An engineer can configure the Visual System Simulator test model 1 to replicate 16, 32 or 64 users in a base station cell by reading in the appropriate orthogonal channel noise simulation (OCNS) file. Each OCNS file is representative of the DPCH information found in table 6.2 section 6.1.1.1 of the base station conformance specifications.

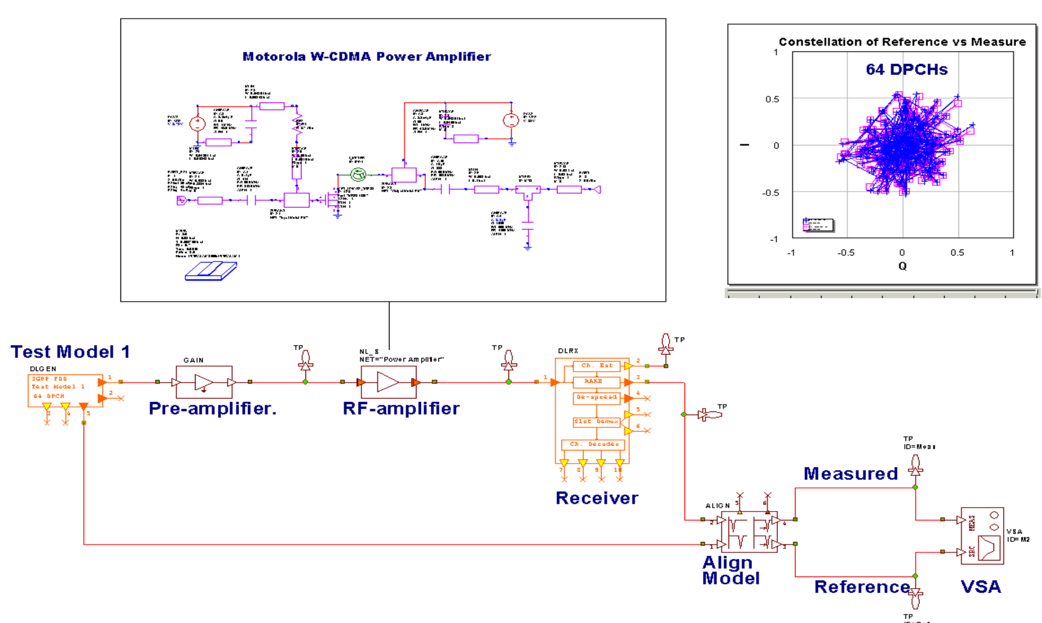

Figure 3: EVM Test Bench

In Figure 3, P_{MAX} is set to 35dBm and the transmit frequency is set to 2140MHz. The oversampling ratio in the test model is manually set to 8 times the 3.84MHz chip rate. In addition, test model 1 uses the primary common control physical channel (CCPCH), SCH, and C-PICH. To reduce the EVM to an absolute minimum, an identical RRC filter characteristic (per specifications) is used in both the transmitter and receiver. The signal of test model 1 is passed through a pre-amplifier to adjust overall output power level, and then passed through the RF amplifier under test. The RF amplifier is designed in AWR;s Microwave Office™ software and is introduced into the system diagram using the VSS nonlinear simulation-based model. The amplifier introduces phase and amplitude distortion, effectively rotating the QPSK constellation around the origin. The receiver performs a channel estimate using the C-PICH signal. The transmitted phase of the pilot is 45-degrees, therefore, by recovering the pilot's phase the receiver can estimate the phase offset introduced by the amplifier and then rotate the constellation to correct the phase offset. The receiver is designed to measure the timing-offset, and adjusts its chip timing-offset to within 1/8th chip of the ideal sampling point. It also decimates the signal to recover the original 3.84MHz chip-rate QPSK signal. The coherently detected chip and the original transmitted chips are then passed through a VSS signal align model to compensate for group delay and gain. The delay compensation is performed by correlating the distorted signal and with the reference signal samples to estimate the required delay correction. The gain adjustment is achieved by using a comprehensive algorithm to appropriately scale the distorted signal relative to the reference signal. Both outputs of the align model, the reference (s_n) and measured (z'_n) samples, are then fed into a VSS vector signal analyzer (VSA). The VSA in conjunction with the built-in VSS EVM measurement are used to make the RMS EVM measurement over 2560 chips. The results of the simulation show that the RMS EVM, whether 16, 32 or 64 channels were generated, was 8.5% +/- 1%. The complimentary cumulative distribution function (CCDF) indicated that the PAR was approximately 8dB. For reference purposes, an EVM simulation using test model 4 revealed an overly optimistic 2%. Evidently, the results of the simulation indicate that the RF amplifier is in compliance with specifications. In short, the simulation results enable the design team to budget EVM with respect to the power amplifier stage.

The simulation tool used in this example also supports the necessary models for handset testing, such as ACLR, as well as the models according to conformance testing for handsets. With these models, users can concentrate on design work rather than studying standards details.

The 3GPP test blocks provided in this solution are compliant with the 3GPP FDD universal mobile telecommunications systems (UMTS) specifications. Integrated circuit and system level solutions can significantly accelerate 3G design by incorporating transistor level effects into high-level simulations. VSS2004 software, which offers an optional 3G design library, provides complete 3GPP simulation and evaluation support for both handset (UE) and base station (node-b) wireless communication equipment.

References:

[1] "3GPP TS25.141" 3GPP FDD Base Station Conformance Testing, section 6.7.1.1; Latest specifications are available at: ftp://ftp.3gpp.org/specs/latest/

[2] ibid, section 6.7.1.2

[3] "TSG-RAN Meeting #22, December 2003, RP-030714" page 2.